TITLE OF THE INVENTION

DATA CONVERSION APPARATUS AND DATA CONVERSION METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the

benefit of priority from the prior Japanese Patent

Application No. 2002-382261, filed December 27, 2002,

the entire contents of which are incorporated herein by

reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a data conversion

apparatus and method which convert m-bit data into

n-bit data.

2. Description of the Related Art

Generally, binary data recorded on an optical disk

is converted (modulated) into a code with a suppressed

DC component. The minimum number of "0" bits between

"1" bits in the converted (modulated) code sequence is

represented by d. The maximum number of "0" bits

between "1" bits is represented by k. The code used

for modulation is called a (d, k) code.

A current DVD (Digital Versatile Disk) employs

a (2, 10) code for modulation. In recent years,

the data playback technology from optical disks has

improved, and a PRML (Partial Response Maximum

Likelihood) technique is employed. Accordingly,

employment of a "d = 1" modulation code suitable for

a high density has been examined.

For example, Jpn. Pat. Appln. KOKAI Publication No. 2000-105981 (reference 1) discloses a technique in which the above-described "d = 1" modulation code is employed, and additionally, a DC suppressing inversion bit is added to the end of a converted code.

In addition, Jpn. Pat. Appln. KOKAI Publication No. 2000-332613 (reference 2) discloses a technique in which the above-described "d = 1" modulation code is employed to convert 4-bit data into 6-bit data.

In the technique disclosed in reference 1, however, since 8-bit data is converted into 12-channel bit data, $2^8 = 256$ or more conversion patterns are necessary. As a result, the conversion table size becomes large, and modulation/demodulation processing (conversion processing) is complicated.

In the technique disclosed in reference 2, since 4-bit data is converted into 6-channel bit data, only $2^4 = 16$ conversion patterns suffice. As a consequence, the conversion table size is small. However, since the conversion table requires four states, the problem of complex modulation/demodulation processing is not solved.

BRIEF SUMMARY OF THE INVENTION

According to an aspect of the present invention, there is provided a data conversion apparatus comprising a storage unit configured to store a

conversion table to convert m-bit data into n-bit data, and a conversion unit configured to convert the m-bit data into the n-bit data by using the conversion table stored in the storage unit,

5   wherein the conversion table contains a plurality of bit conversion codes to convert the m-bit data into the n-bit data,

    the bit conversion code is a code which converts the m-bit data into the n-bit data that allows the

10   minimum number d of consecutive "0" bits between "1" bits,

    a code at an end of at least one of all the bit conversion codes in the conversion table is an inversion bit for DC suppression, and

15   the inversion bit selects one of "0" and "1" in accordance with a predetermined condition.

    According to an aspect of the present invention, there is provided a data conversion method of converting m-bit data into n-bit data, comprising

20   converting the m-bit data into the n-bit data by using a conversion table,

    wherein the conversion table contains a plurality of bit conversion codes to convert the m-bit data into the n-bit data,

25   the bit conversion code is a code which converts the m-bit data into the n-bit data that allows the minimum number d of consecutive "0" bits between

successive "1" bits,

a code at an end of at least one of all the bit conversion codes in the conversion table is an inversion bit for DC suppression, and

5   the inversion bit selects one of "0" and "1" in accordance with a predetermined condition.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification,

10   illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

15   FIG. 1 is a view showing an example of data conversion tables used for data conversion by a data conversion method and apparatus according to one embodiment of the present invention;

FIG. 2 is a table for explaining exceptional cases

20   of data conversion by the data conversion method and apparatus according to one embodiment of the present invention;

FIG. 3 is a graph for explaining various symbols related to trace back DCC control applied to the

25   present invention;

FIG. 4 is a graph for explaining the effects of trace back DCC control applied to the present

invention;

FIG. 5 is a schematic block diagram showing an example of the data conversion apparatus according to the present invention;

FIG. 6 is a table for explaining the run occurrence frequency in data converted by the data conversion method and apparatus according to one embodiment of the present invention;

FIG. 7 is a table showing the evaluation result of the number of times of repetition of fine pattern (2T) in data converted by the data conversion method and apparatus according to one embodiment of the present invention;

FIG. 8 is a graph showing the DSV characteristic evaluation result of data converted by the data conversion method and apparatus according to one embodiment of the present invention; and

FIG. 9 is a table that summarizes the DSV characteristic evaluation result shown in FIG. 8.

DETAILED DESCRIPTION OF THE INVENTION

The embodiment of the present invention will be described below with reference to the accompanying drawing.

FIG. 1 is a view showing an example of conversion tables used for data conversion by a data conversion apparatus and method according to the present invention. The data conversion method and apparatus

of the present invention allow 1 as the minimum number
of consecutive "0" bits between successive "1" bits
(d = 1).   In addition, 4-bit data is converted into
6-bit data by using two (two states) conversion tables
including a fixed length block code that converts 4
bits into 6 bits.   At least one of converted codes has
a DC suppressing inversion bit * at its end.   In the
conversion code shown in FIG. 1, the minimum number k
of consecutive "0" bits between successive "1" bits can
be k = 8.

By using the conversion tables shown in FIG. 1,
4-bit data is converted into 6-bit data.   Accordingly,
the data conversion method and apparatus of the present
invention can obtain the following functions and
effects.

(1) Since the fixed length block code scheme is
employed, modulation/demodulation processing can be
simplified.

(2) The conversion unit of the fixed length block
code is set as small as 4 bits → 6 bits.   In addition,
only two states are set as states after conversion.
With this arrangement, the conversion table size can be
reduced, and modulation/demodulation processing can be
simplified.

(3) The "inversion bit *" is set to the last
channel bits of some conversion codes.   When the bit
of the "inversion bit *" is controlled ("inversion bit

*" = "0" or "1"), DC control can relatively easily be executed.

(4) When pattern replacement processing is executed for a specific pattern after conversion, the 2T repetition frequency in the converted code can be limited.

FIG. 1 is a view showing an example of conversion tables for "4-6 conversion". There can exist 16 patterns of 4-bit data before conversion. Two conversion states (STATE) are present in correspondence with each of the 16 patterns. Each conversion code is assigned the next STATE number to designate the state (STATE) that should be selected for conversion of next data.

Some conversion codes have the "inversion bit *" that is set to the last channel bits. The value of the "inversion bit *" is selected such that the DSV (Digital Sum Value) value for a channel bit data sequence after conversion becomes close to "0". With this method, DC control can be executed in the present invention (this will be described later in detail). The "inversion bit *" is always present at the last channel bit position of the converted code. Since the position where the "inversion bit *" can exist is always known in advance, the value of the "inversion bit *" can relatively easily be determined.

The conversion tables shown in FIG. 1 will be

described below.

(A) Codes after conversion, which start with "0", and in which a run length of "0" channel bits from the start is three or less, are put into a group "STATE 1".

5   (B) Codes except (A), i.e., codes which start with "1" or "0", and in which a run length of "0" channel bits including the start bit is four or more are put into a group "STATE 0".

(C) When the last channel bit of a code after
10   conversion is "1", STATE 1 always should be selected as the next STATE.

As described above, for example, the present invention is based on a modulation (conversion) scheme that satisfies d = 1. The conversion code (modulation
15   scheme) with d = 1 inhibits a run of "1" bits as a code sequence after modulation (conversion). In this modulation scheme, at least one "0" bit must be inserted between "1" bits. In the above structure, when "1" exists as the last channel bit of a converted
20   code, as indicated by (C), STATE 1 is selected. In STATE 1, "0" always exists at the start of the next conversion code, as indicated by (A), so that the conversion rule "d = 1" is automatically satisfied. Hence, in the present invention, any new mechanism
25   need not be introduced to inhibit a run of "1" bits. With only the characteristic features (A) to (C), the conversion rule "d = 1" can be satisfied. For this

reason, conversion processing can be simplified.

The conversion tables shown in FIG. 1 also will be described below.

(D) The channel bit immediately before the inversion bit is always "0". Hence, even when "1" is selected as the inversion bit, the code never have a run of two "1" bits including the channel bit immediately before the inversion bit. Without introducing any new mechanism to inhibit a run of "1" bits, the conversion rule "d = 1" can be satisfied. For this reason, conversion processing can be simplified.

(E) When the number of consecutive "0" bits immediately before the inversion bit is three or less, STATE 0 is selected for the next conversion to increase the number of consecutive "0" bits.

(F) When the number of consecutive "0" bits immediately before the inversion bit is four or more, either STATE can be selected.

With the description (E) and (F), the DC control effect can be improved.

In data recorded on an optical disk, the local recording density is high in a place where "2T" is repeatedly recorded. For this reason, the amplitude of a playback signal that is played back from the place where "2T" is repeatedly recorded is very small, and a signal detection error readily occurs. In the

present invention, to increase the signal detection
reliability, the "2T" signal repetition frequency in
a channel bit sequence after modulation is limited,
as shown in FIG. 2. More specifically, pattern

5   replacement processing is executed for a specific
pattern after conversion, thereby limiting the 2T
repetition frequency in the converted code.

When STATE 0 is employed for data "6" before
conversion in FIG. 1, and STATE 1 is employed for

10   data "5" before conversion, "2T" is repeated in the
converted data. When data containing two data "6"
before conversion is converted by employing STATE 0 of
the conversion tables shown in FIG. 1, the converted
code is "101010101010". When data containing two data

15   "5" before conversion is converted by employing STATE 1
of the conversion tables shown in FIG. 1, the converted
code is "010101010101". In these cases, "1" is
generated six times in the 12-channel bit code after
conversion. If the "1" occurrence frequency becomes

20   high as in the above-described cases, another
conversion code is assigned, as shown in FIG. 2.

More specifically, data containing two data "6"
before conversion should originally be converted into
"101010101010". However, the data is converted into

25   "100100" + "00000*". In addition, STATE 0 is
designated as STATE for the next conversion. Data
containing two data "5" before conversion should

originally be converted into "010101010101". However, the data is converted into "010100" + "00000∗".
In addition, STATE 1 is designated as STATE for the next conversion.

As the DC suppressing inversion bit ∗ that exists at the end of some conversion codes in the conversion tables shown in FIG. 1, "0" or "1" is selected in accordance with a predetermined condition. The selection method will be described below.

In data converted by the data conversion apparatus and method of the present invention, the DC component is suppressed by a trace back method. First, various symbols related to the trace back DCC control method will be defined with reference to FIG. 3.

1. Definition of Symbols

DCC_n: the position of the nth preceding DCC code from the current position (latest code)

DSV: the DSV value at the current position

POL: the inversion state at the current position (whether the number of times of inversion is even or odd)

$DSVP_n$: the positive DSV peak value from the current position to DCC_{n+1}

$DSVM_n$: the negative DSV peak value from the current position to DCC_{n+1}

$DSVS_n$: the DSV value of a section until DCC_n based on DCC_{n+1}

DSVSPn: the positive DSV peak value of a section until DCCn based on DCCn+1

DSVSMn: the negative DSV peak value of a section until DCCn based on DCCn+1

5   DCCIn: the inversion/non-inversion state of DCCn

2. Section Value Calculation Method

The section value can easily be calculated by fixing the polarity of a DCC bit. However, a today's program calculates the section value on the basis of

10   the state after DCC processing without prefetching.

DSV calculation is done at a DCC bit position in a DCC code (including a SYNC). In other codes, the calculation is done at the LSB position. However, since the DCC bit is fixed by the LSB, correction

15   processing is easy. The hold of a peak value is also calculated on the basis of the same standard.

The procedures of the trace back DCC control method will be described next with reference to FIG. 3.

3. Procedures of Trace Back DCC Control Method

20   (1) The DSV peak values (DSVP1 and DSVM1) in the section from DCC0 to DCC2 are obtained.

Peak calculation is executed retrospectively from DSV and POL. That is, DSVP1 is obtained from DSVS0, DSVS1, DSVPS0, DSVPS1, DCCI0, and DCCI1. DSVM1 is

25   obtained from DSVS0, DSVS1, DSVMS0, DSVMS1, DCCI0, and DCCI1.

(2) DSV peak values when DCC2 and DCC1 are

simultaneously inverted are obtained.

When the sections of DCC2 and DCC1 are in the same inversion states as in section value calculation, the peak values are obtained by subtracting 2 × DSVS1 from DSVP1 and DSVM1. When the sections of DCC2 and DCC1 are in inversion states reverse to those in section value calculation, the peak values are obtained by adding 2 × DSVS1 to DSVP1 and DSVM1.

(3) Execution of simultaneous inversion processing is determined from the four DSV peak values.

The absolute values of the four DSV peak values are calculated and compared.

Simultaneous inversion processing is selected such that the peak having the largest absolute value is eliminated.

(4) DSV, DCCI1, and DCCI2 are updated in accordance with the selection result.

(5) DSVP2 and DSVM2 in the section from DCC0 to DCC3 are obtained next in a similar way.

(6) The DSV peak values are compared with DSV peak values obtained when DCC3 and DCC2 are simultaneously inverted.

(7) Execution of simultaneous inversion processing is determined.

(8) DSV, DCCI2, and DCCI3 are updated in accordance with the selection result.

(9) The above processing is repeated while

increasing the length of the calculation section until a predetermined number of DCC codes.

The above-described processing is executed every time a DCC code or a SYNC is detected.

4. Example of DCC Processing

FIG. 4 shows an example of effects by the above processing.

DSV change 1 shown in FIG. 4 indicates a DSV change in DCC processing without prefetching. When trace back DCC processing is executed for this DSV change, the following operation is executed.

(1) Check of Simultaneous Inversion States of DCC2 and DCC1

Since the positive DSV peak becomes large after simultaneous inversion, the simultaneous inversion processing is not executed.

(2) Check of Simultaneous Inversion States of DCC3 and DCC2

Since the DSV peak values do not change, the simultaneous inversion processing can be either executed or omitted. In this example, simultaneous inversion is not executed.

(3) Check of Simultaneous Inversion States of DCC4 and DCC3

When the simultaneous inversion processing is not executed, the positive DSV peak is maximum. Hence, simultaneous inversion processing of DCC4 and DCC3 is

executed.   Only the DSV change in the sections of DCC4
and DCC3 is inverted (DSV change 2 shown in FIG. 4).
The DSV from DCC3 is wholly shifted in the negative
direction by 2 × DSVS3 (DSV change 3 shown in FIG. 4).

5   As a result, the DSV peak values are suppressed.
5. Example of Circuit Arrangement

           FIG. 5 is a block diagram showing the schematic
arrangement of the data conversion apparatus according
to the present invention.   In other words, the data
10   conversion apparatus has circuits necessary for trace
back DCC.   As shown in FIG. 5, the data conversion
apparatus comprises a code table/sync table 1,
modulation/sync insertion processing section 2,
frame buffer 3, bit inversion processing section 4,
15   NRZI processing section 5, section DSV/section peak
calculation section 6, DCC buffer 7, and trace back
determination section 8.

           The code table/sync table 1 stores the conversion
tables shown FIG. 1 and sync codes.   The modulation/
20   sync insertion processing section 2 converts
(modulates) input data on the basis of the conversion
tables shown in FIG. 1.   More specifically, the
modulation/sync insertion processing section 2 converts
input 4-bit data into 6-bit data and inserts a sync
25   code every predetermined data length.   The code
table/sync table 1 also stores information that limits
the "2T" signal repetition frequency shown in FIG. 2.

With this information, the "2T" signal repetition frequency is limited.

The frame buffer 3 can buffer, e.g., several sync frames. One sync frame is constituted by a sync code and converted data. Only one data sequence after temporary determination is stored in the frame buffer 3. To save the capacity of the frame buffer 3, a limitation on the maximum number of frames may be added to the section of trace back.

The section DSV/section peak calculation section 6 calculates a section DSV and section peak, as described above. The DCC buffer 7 stores the DCC positions, inversion states, and section values. The trace back determination section 8 executes trace back determination on the basis of the information stored in the DCC buffer 7. That is, the trace back determination section 8 executes addition/subtraction and absolute value comparison for the respective values in the DCC buffer 7.

The bit inversion processing section 4 inverts the DC suppressing inversion bit * in accordance with the trace back determination result of the trace back determination section 8. That is, the DC suppressing inversion bit * is set to "1" or "0". The modulation table is unnecessary for inversion processing after trace back determination.

The NRZI processing section 5 outputs an NRZI

pattern which inverts the output in accordance with
a "1" bit and holds the output in accordance with a
"0" bit.

FIG. 6 is a table for explaining the run
occurrence frequency in data converted by the data
conversion method according to the present invention.
As shown in FIG. 6, the occurrence frequency is highest
for 2T. The second highest occurrence frequency is for
3T. The occurrence frequency distribution shown in
FIG. 6 corresponds to the result of 2T repetition
control shown in FIG. 2. When the control is executed,
the 2T occupation ratio (22.5%) decreases and almost
equals the 3T occupation ratio (22.1%).

FIG. 7 is a table showing the evaluation result
of the number of times of repetition of fine pattern
(2T) in data converted by the data conversion method
according to the present invention. As is apparent
from FIG. 7, when the 2T repetition control shown in
FIG. 2 is executed, the repetition frequency of two 2Ts
(24.5%) is much lower than the repetition frequency of
one 2T (60.4%).

FIGS. 8 and 9 are views showing the DSV
characteristic evaluation result of data converted by
the data conversion method according to the present
invention. As is apparent from FIGS. 8 and 9, when
the above-described trace back DCC control is executed,
the distribution is small, and the DSV value converges

to 0.

As has been described above, in the present invention, the following functions and effects are obtained by employing the "d =1" modulation method.

5   (1) The conversion table can be simplified (the conversion table size can be reduced), and conversion processing can be facilitated. In addition, since the conversion table is simple, highs-speed conversion can be executed.

10   (2) DC control can be executed by a simple method. Hence, highly accurate playback can be executed.

    (3) The 2T repetition frequency can be limited, and playback signal detection can be stabilized. Hence, highly accurate playback can be executed.

15   Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various

20 modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.